REMARKS

Claims 1-6 and 8-25 are pending in the current application. Claims 1 and 22 are amended by this response. Support for these amendments may be found in the specification, figures and claims as originally filed. It is believed that no new matter has been entered through these amendments and entry is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

I. Claims 1-6, 8-10, 12-19, and 24-25

Claims 1-6, 8-10, 12-19, and 24-25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,852,065 to Baddiley (hereinafter "Baddiley") in view of U.S. Patent Application Publication No. 2004/0111567 to Anderson et al. (hereinafter "Anderson"). These rejections are respectfully traversed and reconsideration is requested in light of the remarks below.

A. Neither Baddiley nor Anderson, alone or in combination, teach or fairly suggest "a plurality of different and *non-sequential* groups of memory cells," as recited in claim 1.

While Baddiley does not explicitly teach a "group" or any other collection of memory cells, the Examiner appears to conclude that a group of memory cells exists because the buffers 20, 21 are able to handle different word sizes. (See Office Action at paragraphs 32, 34). In paragraph 32 of the Office Action, the Examiner appears to equate the collection of memory cells that store a data word in Baddiley to a group of memory cells because, according to the Examiner, if a 32-bit word format were used, each word would be stored in a group of memory cells spanning 4 rows and 8 columns. Assuming that the Examiner is correct that a 32-bit word would be stored in 4 rows and 8 columns, which Applicants do not (as will be explained below), the rows and columns of memory cells containing the 32-bit word would be sequential, in contrast to "a plurality of different and *non-sequential* groups of memory cells," recited in claim 1.

Baddiley explicitly discloses sequentially reading from and writing to memory cells. (See Baddiley, column 5, lines 27-68). For example, Baddiley teaches that "successive bytes are written into successive byte locations." (Baddiley, column 5, lines 36-37). Summarizing the data transfer operations, Baddiley discloses that "in summary, data is written into the buffer as a *sequence* of planes parallel to the x-y plane, and is then read out as a *sequence* of planes parallel to the y-z plane." (emphasis added) (Baddiley, column 5, lines 63-65).

In contrast to the sequential access of memory cells disclosed in Baddiley, the present application discloses accessing memory cells that are non-sequentially distributed throughout the memory matrix. Specifically, a plurality of data memory cells is arranged in the form of a matrix having rows and columns. The data memory cells are further arranged in groups within the matrix. In particular, page 12 of the specification of the present application discloses four groups: A, B, C, and D. As shown by Table 1 of the present application, members of a given group are located within different rows and different columns and are distributed *non-sequentially* among the rows and columns. For example, with reference to Table 1 of the present application, the members of group A span diagonally across the memory matrix. Such a non-sequential distribution of groups across rows and columns is simply not taught or fairly suggested by Baddiley, which simply transferred data into and out of RAM components sequentially.

Accordingly, Baddiley fails to teach or fairly suggest "a plurality of different and *non-sequential* groups of memory cells," recited in claim 1. Anderson is merely cited in the Office Action because it allegedly teaches multi-port memory devices able to read and write data in a single clock cycle. However, Anderson does not assist in teaching or fairly suggesting "a plurality of different and *non-sequential* groups of memory cells." Thus, neither Baddiley nor Anderson, alone or in combination, teach or fairly suggest this limitation of claim 1. Accordingly, claim 1 and all claims that depend therefrom (e.g., claims 2-6, 8-10, 12-19, and 24-25) are patentable over Baddiley in view of Anderson.

B. Neither Baddiley nor Anderson, alone or in combination, teach or fairly suggest each group of memory cells "having members of the group located in different rows and in different columns of the matrix."

As noted above, the Examiner appears to equate the collection of memory cells that store a data word in Baddiley to a group of memory cells. (See Office Action at paragraph 32). According to the Examiner, if a 32-bit word format were used, each word would be stored in a group of memory cells spanning 4 rows and 8 columns. Applicants respectfully disagree.

Referring to FIG. 2 of Baddiley, data reorganization unit 14 includes 8 rows and 8 columns of 512-bit memory cells. A nine-bit address A0-A8 allows a specific bit location in each 512-bit memory cell to be selected, which permits the same bit position in each of the 512-bit memory cells to be accessed in parallel.

In the context of a write operation, a 32-bit input data word is received by the data reorganization unit 14 on the 32-bit wide path 23. The 32-bit input word is multiplexed down via multiplexing switch 25 to an 8-bit wide path 24, which carries the 8-bit portion of the 32-bit input word to the buffers 20, 21. The control signals WA5, WA6 control the multiplexing switch 25 to determine which 8-bit portion of the 32-bit input word is currently output on the 8-bit wide path 24. The control signals W0,W1,W2 produce a write enable signal that selects one row of bit positions into which the 8-bit portion of the 32-bit input word is written.

Referring now to FIG. 4, the address signals A0-A8 and the control signals WA5,WA6,W0,W1,W2 are generated by the counter 40. Of particular importance, multiplexing control signals WA5 and WA6 correspond to bits 0 and 1 of counter 40 and row selection control signals W0,W1,W2 correspond to bits 7-9 of counter 40.

By way of example, if a 32-bit input word is provided on input path 23 when the counter outputs 00000000000, the multiplexing control signals WA5 and WA6 would be 00, causing the first 8-bit portion of the 32-bit input word to be provided on path 24. The row selection control signals W0,W1,W2 would be 000, causing the first 8-bit portion of the 32-bit input word to be input to the first row of the buffer 20. When the counter advances to output 00000000001, the

multiplexing control signals WA5 and WA6 would be 01, causing the second 8-bit portion of the 32-bit input word to be provided on path 24. The row selection control signals W0,W1,W2 would still be 000, causing the second 8-bit portion of the 32-bit input word to also be input to the first row of the buffer 20. When the counter advances to output 00000000010, the multiplexing control signals WA5 and WA6 would be 10, causing the third 8-bit portion of the 32-bit input word to be provided on path 24. The row selection control signals W0,W1,W2 would still be 000, causing the third 8-bit portion of the 32-bit input word to also be input to the first row of the buffer 20. When the counter advances to output 00000000011, the multiplexing control signals WA5 and WA6 would be 11, causing the fourth 8-bit portion of the 32-bit input word to be provided on path 24. The row selection control signals W0,W1,W2 would still be 000, causing the fourth 8-bit portion of the 32-bit input word to also be input to the first row of the buffer 20.

As can be seen by this example, a 32 bit word would not be stored in 4 rows and 8 columns, as the Examiner has asserted, but instead, would be stored in 8 sequential columns and only 1 row. Thus, Baddiley does not teach or fairly suggest each group of memory cells "having members of the group located in different rows and in different columns of the matrix," as recited in claim 1. Anderson is merely cited in the Office Action because it allegedly teaches multi-port memory devices able to read and write data in a single clock cycle. However, Anderson does not assist in teaching or fairly suggesting each group of memory cells "having members of the group located in different rows and in different columns of the matrix." Thus, neither Baddiley nor Anderson, alone or in combination, teach or fairly suggest this limitation of claim 1. Accordingly, claim 1 and all claims that depend therefrom (e.g., claims 2-6, 8-10, 12-19, and 24-25) are patentable over Baddiley in view of Anderson.

C. Neither Baddiley nor Anderson, alone or in combination, teach or fairly suggest "an enabling means having dedicated strobe connections to each of the plurality of groups of memory cells and being arranged to exclusively enable memory cells belonging to a selected one of the plurality of groups, as determined by the size of the data items being transferred"

Baddiley simply contains no teaching or fair suggestion of "an enabling means having dedicated strobe connections to each of the plurality of groups of memory cells and being arranged to exclusively enable memory cells belonging to a selected one of the plurality of groups, as determined by the size of the data items being transferred." As stated above, Applicants do not agree that Baddiley discloses a group of memory cells. Further, Baddiley certainly does not disclose selectively enabling particular groups of data memory cells.

Claim 1 recites "an enabling means having dedicated strobe connections to each of the plurality of *groups*." The strobe connections to each of the plurality of groups is distinct from connections to each individual memory cell because strobe connections to each group permits a given group to be *selectively enabled*, while the remainder of the groups remain disabled. Further, the choice of which group to enable is made *in response* to the size of the data items being transferred.

By way of example, when there are data items of a first size, a first group of memory cells are enabled via the strobe connections while the rest of the groups of memory cells are disabled. When there are data items of a second size, a second group of memory cells are enabled via the strobe connections while the rest of the groups of memory cells are disabled. Thus, the size of the words to be transferred affects specifically which memory cells are enabled by the enabling means. In other words, different sizes of words to be transferred cause a different *group* of memory cells *to be enabled*.

Further, selectively enabling a group of data memory cells increases the overall speed of data transfer without facing associated wiring costs/constraints because memory cells are exclusively enabled as determined by the size of the data items being transferred. Accordingly, the disabled memory cells in a corner-turning function can be ignored. Neither the desirability of increasing the overall speed of data transfer nor the way in which it can be realized is taught or fairly suggested by Baddiley. Specifically, Baddiley teaches maintaining a constant speed of data transfer (e.g., by increasing the clock rate by which the data buffer operates by a factor of four). (Baddiley, column 1, line 64 – column 2, line 21). Instead, Baddiley is focused on reducing the size of the buffer store and the number of memory components. Accordingly,

Baddiley does not suggest increasing the overall data transfer rate, and even if it did, a person of ordinary skill in the art at the time of the invention would likely increase the clock rate, instead of group data memory cells.

Thus, Baddiley does not teach or fairly suggest "an enabling means having dedicated strobe connections to each of the plurality of groups of memory cells and being arranged to exclusively enable memory cells belonging to a selected one of the plurality of groups, as determined by the size of the data items being transferred." Anderson is merely cited in the Office Action because it allegedly teaches multi-port memory devices able to read and write data in a single clock cycle. However, Anderson does not assist in teaching or fairly suggesting "an enabling means having dedicated strobe connections to each of the plurality of groups of memory cells and being arranged to exclusively enable memory cells belonging to a selected one of the plurality of groups, as determined by the size of the data items being transferred." Thus, neither Baddiley nor Anderson, alone or in combination, teach or fairly suggest this limitation of claim 1. Accordingly, claim 1 and all claims that depend therefrom (e.g., claims 2-6, 8-10, 12-19, and 24-25) are patentable over Baddiley in view of Anderson.

D. Neither Baddiley nor Anderson, alone or in combination, teach or fairly suggest each group of memory cells "being individually addressable to effect transfer of a data word thereto"

For at least the same reasons set forth in section C above as to why Baddiley does not teach or fairly suggest "an enabling means having dedicated strobe connections to each of the plurality of *groups*," Baddiley also does not teach or fairly suggest each group of memory cells "being individually addressable to effect transfer of a data word thereto," as recited in claim 1. Anderson is merely cited in the Office Action because it allegedly teaches multi-port memory devices able to read and write data in a single clock cycle. However, Anderson does not assist in teaching or fairly suggesting each group of memory cells "being individually addressable to effect transfer of a data word thereto." Thus, neither Baddiley nor Anderson, alone or in combination, teach or fairly suggest this limitation of claim 1. Accordingly, claim 1 and all claims that depend therefrom (e.g., claims 2-6, 8-10, 12-19, and 24-25) are patentable over

Baddiley in view of Anderson.

E. Neither Baddiley nor Anderson, alone or in combination, teach or fairly suggest each group of memory cells being "a subgroup of the total number of memory cells in the matrix"

Baddiley describes a data reorganization apparatus in which data is transferred in or out of the memory using *all* the available memory cells. As stated in Column 4, lines 56-59 of Baddiley, "when the counter reaches its maximum count value (all ones) it stops and produces a signal FULL which indicated that the buffer which is currently being used for writing is *now full*" (emphasis added). In contrast to utilizing the entire buffer, as disclosed in Baddiley, the present application teaches only utilizing a sub-group of memory cells at one time.

Accordingly, Baddiley does not teach or fairly suggest each group of memory cells being "a subgroup of the total number of memory cells in the matrix," as recited in claim 1. Anderson is merely cited in the Office Action because it allegedly teaches multi-port memory devices able to read and write data in a single clock cycle. However, Anderson does not assist in teaching or fairly suggesting each group of memory cells being "a subgroup of the total number of memory cells in the matrix." Thus, neither Baddiley nor Anderson, alone or in combination, teach or fairly suggest this limitation of claim 1. Accordingly, claim 1 and all claims that depend therefrom (e.g., claims 2-6, 8-10, 12-19, and 24-25) are patentable over Baddiley in view of Anderson.

F. There is no motivation to combine Baddiley and Anderson

The Examiner cites Baddiley as disclosing all of the limitations of claim 1, except "a single transfer operation comprising a single clock cycle." To address this deficiency of Baddiley, the Examiner cites Anderson as teaching a multi-port memory device able to read and write data in a single clock cycle. The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made for the multi-ported memory of Baddiley to be able to perform read and write operations in one clock cycle because Anderson

teaches multi-port memories performing read and write accesses to data in one clock cycle. Applicants respectfully disagree.

It would not have been obvious to combine Baddiley and Anderson. The claim 1 limitation of transferring data in a single clock cycle, as allegedly disclosed by Anderson, is inherently incompatible with the data reorganization apparatus of Baddiley. The way that data is written *sequentially* to and from the memory of Baddiley ensures that even if data transfer in a single clock cycle were desirable, it could not be achieved with the system of Baddiley. In fact, the system disclosed by Baddiley requires four clock cycles to transfer a single 32-bit word. Quadrupling the clock speed to four times the input data word rate, as disclosed by Baddiley, in order to compensate for a smaller memory buffer, teaches away from "a single transfer operation comprising a single clock cycle," as recited in claim 1 of the present application. Accordingly, claim 1 and all claims that depend therefrom (e.g., claims 2-6, 8-10, 12-19, and 24-25) are patentable over Baddiley in view of Anderson.

II. Claim 11

Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Baddiley in view of Anderson, and further in view of U.S. Patent No. 6,781,898 to Kim et al. (hereinafter "Kim"). This rejection is respectfully traversed.

Claim 11 depends from claim 1. As noted above, Baddiley in view of Anderson do not teach or fairly suggest all of the limitations of claim 1. Kim was narrowly cited as including the feature of detecting and skipping defective rows in a memory. However, Kim does not assist Baddiley and Anderson in teaching or fairly suggesting all of the limitations of claim 1. Therefore, the combination of Baddiley, Anderson, and Kim do not teach or fairly suggest all of the limitations of claim 1. Accordingly, claim 11 is patentable over Baddiley in view of Anderson, and further in view of Kim.

III. Claims 20-23

Claims 20-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Baddiley in view of Anderson, and further in view of U.S. Patent No. 5,581,773 to Glover (hereinafter "Glover"). These rejections are respectfully traversed.

Claims 20-21 depend from claim 1. As noted above, Baddiley in view of Anderson do not teach or fairly suggest all of the limitations of claim 1. Glover was narrowly cited as disclosing the feature of a masking register. However, Glover does not assist Baddiley and Anderson in teaching or fairly suggesting all of the limitations of claim 1. Therefore, the combination of Baddiley, Anderson, and Glover do not teach or fairly suggest all of the limitations of claim 1. Accordingly, claims 20-21 are patentable over Baddiley in view of Anderson, and further in view of Glover.

Independent claim 22 has been amended to recite similar features as claim 1 and is believed to be allowable for at least the same reasons noted previously with respect to claim 1.

Claim 23 depends from claim 22 and is allowable for at least the same reason.

Conclusion

Applicants respectfully submit that the currently pending claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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